AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) Phase locked loop charge pump comprising:

a drain node; and

at least a cascode transistor for limiting the variation of the voltage of said drain node,

wherein an intermediate switch transistor is placed between the drain node and the cascode transistor.

2. (Currently Amended) The charge pump of claim 1, wherein said drain node is a first node and said cascode transistor is a first cascode transistor, said charge pump further comprises~~ing a first node,~~ a second node~~;~~, a branch connecting the first node with the second node, said branch comprising the ~~a~~ first cascode transistor and a second cascode transistor, a first switch transistor is coupled across from the first cascode transistor, and a second switch transistor coupled across from the second cascode transistor, further comprising ~~an~~ the intermediate switch transistor between ~~the drain node~~ one of the first node and the second node, and one of the first~~a~~ cascode transistor and the second cascode transistor, coupled across from one of the first switch transistor and the second switch transistor.

3. (Currently Amended) The charge pump of claim 2, wherein said intermediate switch transistor is a first intermediate switch transistor, and said charge pump further comprisesing ~~two~~ a second intermediate switch transistors, wherein the ~~a~~ first intermediate transistor is between the first node and the first cascode transistor, said first intermediate transistor being coupled across from the first switch transistor, and wherein the second intermediate switch transistor being between the second node and the second cascode transistor, said second intermediate transistor being coupled across from the second switch transistor.

4. (Currently Amended) The charge pump of claim 3, wherein the first switch transistor coupled across from the first cascode transistor and/or the second switch transistor coupled across from the second cascode transistor is connected to a further cascode transistor coupled across from the first and/or second cascode transistor.

5. (Currently Amended) The charge pump of claim 4, wherein the further cascode transistor is a first additional cascode transistor and wherein the first switch transistor coupled across from the first cascode transistor and the~~a~~ first ~~further~~ additional cascode transistor form a dummy branch coupled across from the first cascode transistor and the first intermediate transistor, said dummy branch having connections so as to be controlled by the complement signal of the signal controlling the first intermediate transistor and/or the second switch transistor coupled across from the second cascode transistor and a second ~~further~~ additional cascode transistor form ~~a~~ the dummy branch coupled across from the second cascode transistor and the second intermediate

transistor, said dummy branch having connections so as to be controlled by the complement signal of the signal controlling the second intermediate switch transistor.

6. (Previously Presented) An electronic circuit comprising a charge pump according to claim 1.

7. (Previously Presented) An integrated circuit comprising a charge pump according to claim 1.

8. (Previously Presented) A phase locked loop charge pump comprising:

a drain node;

a first cascode transistor to limit the variation of the voltage of said drain node;

a first intermediate switch transistor positioned between said drain node and said first cascode transistor; and

a dummy branch with a second cascode transistor connected to a second intermediate switch transistor,

wherein said second intermediate switch transistor is positioned between said first node and said second cascode transistor.

9. (New) The charge pump of claim 1, wherein said drain node is a first node and said cascode transistor is a first cascode transistor, said charge pump further comprises:

a second node;

a branch connecting the first node with the second node, wherein the branch comprises the first cascode transistor and a second cascode transistor, a first switch transistor across from

the first cascode transistor, and a second switch transistor across from the second cascode transistor, and wherein the intermediate switch transistor is between one of the first node and the second node, and one of the first cascode transistor and the second cascode transistor, and the intermediate switch transistor is across from one of the first switch transistor and the second switch transistor.

10. (New) The charge pump of claim 9, wherein said intermediate switch transistor is a first intermediate switch transistor, and said charge pump further comprises:

a second intermediate switch transistor,

wherein the first intermediate transistor is between the first node and the first cascode transistor, and is across from the first switch transistor, and

wherein the second intermediate switch transistor is between the second node and the second cascode transistor and is across from the second switch transistor.

11. (New) The charge pump of claim 10, wherein the first switch transistor is across from the first cascode transistor and/or the second switch transistor is across from the second cascode transistor and wherein the first switch transistor and/or the second switch transistor is connected to a further cascode transistor across from the first and/or second cascode transistor.

12. (New) The charge pump of claim 11, wherein the further cascode transistor is a first additional cascode transistor, and wherein the first switch transistor across from the first cascode transistor and the first additional cascode transistor form a dummy branch, the dummy branch is

across from the first cascode transistor and the first intermediate transistor, and the dummy branch has connections so as to be controlled by the complement signal of the signal controlling the first intermediate transistor, and/or the second switch transistor across from the second cascode transistor and a second additional cascode transistor form the dummy branch, the dummy branch is across from the second cascode transistor and the second intermediate transistor, said dummy branch has connections so as to be controlled by the complement signal of the signal controlling the second intermediate switch transistor.